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IN THE CLAIMS

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please **AMEND** claims in accordance with the following:

Please **CANCEL** claims 14 and 17.

1. (CURRENTLY AMENDED) A method comprising:

transferring a write packet from a first node to a second node, when a plurality of nodes, including the first node, the second node and a third node, connect by a bus but not connected in a ring form and the plurality of nodes constitute an IEEE 1394 topology, the write packet having an identifier storing identification information which indicates addressee of data stored in data portion of the write packet or indicates that the data portion of the write packet includes a blank data portion;

determining at a link layer processor of the second node whether a received packet is the write packet;

checking at an identification circuit of the second node the identification information of the identifier of the received write packet and determining whether data stored in the data portion of the write packet can be replaced with another data stored in the second node and to be addressed to the third node;

storing data addressed to the third node and to be written in a data portion of a packet, in the data portion of the write packet at the second node in accordance with the checking result, wherein said storing data includes replacing the data stored in the data portion of the write packet with said another data; and

transferring the write packet from the second node to the third node.

2. (PREVIOUSLY PRESENTED) The packet transfer method according to claim 1, wherein the write packet comprises a blank data portion for storing the data.

3. (PREVIOUSLY PRESENTED) The packet transfer method according to claim 1,

wherein the first node has information indicating that a plurality of the second nodes substantially simultaneously transfer packets to a plurality of the third nodes, and the write packet transferring comprises transferring a plurality of write packets to the plurality of the second nodes based on the information.

4. (CURRENTLY AMENDED) The packet transfer method according to claim 1, wherein the write packet includes a header portion and a data portion, and ~~wherein the header portion stores~~ the identification information ~~indicating whether the data portion is blank~~ is arranged in the data portion of the write packet.

5. (PREVIOUSLY PRESENTED) A method of transferring packets between a plurality of nodes including a first node, a second node, and a third node connected by a bus but not connected in a ring form, the method comprising:

transferring a write packet from the first node to the second node;

storing data to be written in a data portion of a packet addressed to the third node in the data portion of the write packet at the second node; and

transferring the write packet from the second node to the third node,

wherein the write packet transferring comprises transferring from the first node to the second node a guide packet that stores guide information indicating a state of the write packet, before the first node transfers the write packet to the second node, and

wherein the data storing by the second node comprises writing as the guide information of the guide packet information indicating that the data has been written to the write packet by the second node.

6. (PREVIOUSLY PRESENTED) The packet transfer method according to claim 1, further comprising:

transferring a data packet from the first node to the second node;

processing the data stored in the data packet at the second node; and

transferring the data packet including the processed data to the third node, wherein the write packet transferring is performed after the data packet transferring.

7. (PREVIOUSLY PRESENTED) The packet transfer method according to claim 1, wherein the write packet transferring comprises transferring the write packet from the first node

to the second node at predetermined time periods.

8. (PREVIOUSLY PRESENTED) The packet transfer method according to claim 1, further comprising padding the data stored in the write packet so that the data amount is substantially same as the data storage capacity of the write packet.

9. (PREVIOUSLY PRESENTED) A method of transferring packets between a plurality of connected nodes including a first node, a second node, and a third node, the first node, the second node, and the third node not connected in a ring form, the method comprising:

transferring a first packet storing first data from the first node to the second node;

processing the first data stored in the first packet and temporarily storing the processed first data at the second node;

transferring a second packet storing second data from the first node to the second node;

rewriting the second data stored in the second packet with the processed and temporarily stored first data at the second node; and

transferring the second packet including the processed first data to the third node.

10. (CURRENTLY AMENDED) A packet transfer control circuit, comprising:

a link layer processor as a first node to determine whether a received packet is a write packet, when a plurality of nodes, including the first node, a second node and a third node, are not connected in a ring form and the plurality of nodes constitute an IEEE 1394 topology, wherein the write packet has an identifier storing identification information which indicates addressee of data stored in data portion of the write packet or indicates that the data portion of the write packet includes a blank data portion;

an identification circuit connected to the link layer processor ~~to identify whether a data portion of the write packet received from the second node connected to the first node is blank~~ to check the identifier of the write packet received from an upstream node and determine whether data stored in the data portion of the write packet can be replaced with another data stored in the packet transfer control circuit and to be addressed to a downstream node; and

a host processor connected to the identification circuit to ~~determine whether data can be written to the data portion of the write packet, when the data portion of the write packet is blank according to the identifying by the identification circuit~~ store data addressed to the downstream node to be written in a data portion of a packet, in the data portion of the received write packet in

accordance with the checking result of the identification circuit, wherein said storing data includes replacing the data stored in the data portion of the received write packet with said another data, and transferring the write packet to the ~~third~~ downstream node.

11. (PREVIOUSLY PRESENTED) The packet transfer control circuit according to claim 10, wherein the host processor pads the data stored in the write packet until the data amount is substantially same as data storage capacity of the data portion of the write packet.

12. (CURRENTLY AMENDED) A packet transfer control circuit incorporated in a first node to transfer a packet to ~~a second node and a third node~~ a plurality of other nodes where one of said plurality of other nodes is a downstream node from the first node and one of said plurality of nodes is an upstream node from the first node, in which the first node, ~~the second node, and the third node~~ and the plurality of other nodes are not connected in a ring form, and the first node and the plurality of other nodes, ~~second and third nodes~~ are among a plurality of nodes constituting an IEEE 1394 topology, the packet includes a data portion for storing data, ~~the second node is downstream from the first node, and the third node is upstream from the first node,~~ the first node control circuit comprising:

a processor to perform a multiplex transfer by processing data, which is addressed to the ~~third~~ downstream node and stored in a data portion of a packet received from the ~~second~~ upstream node, temporarily retaining the processed data addressed to the ~~third~~ downstream node, and rewriting data stored in a data portion of a packet received from the ~~second~~ upstream node with the temporarily retained processed data, if the data stored in the data portion of the packet received from the ~~second~~ upstream node is addressed to the ~~third~~ downstream node wherein the processor checks an identifier of a write packet received from the upstream node and determines whether data stored in data portion of the write packet can be replaced with the temporarily retaining processed data addressed to the downstream node and replaces the data stored in the data portion of the received write packet with the temporarily retaining processed data in accordance with the checking result.

13. (CURRENTLY AMENDED) A packet transfer control circuit, comprising:

a processor as first node transferring a plurality of packets determinable at a link layer processor as write packets, the data portion of which is blank, to each of second and third nodes, when a plurality of nodes, including the first, second and third nodes, are not connected

in a ring form and the plurality of nodes constitute an IEEE 1394 topology, based upon information indicating that the second and third nodes substantially simultaneously store data in the data portion of the write packets received from the first node, wherein the processor checks an identifier of each write packet received from an upstream node and determines whether data stored in data portion of each write packet can be replaced with another data stored in the packet transfer control circuit and to be addressed to the second and third nodes and replaces the data stored in the data portion of each write packet with the another data in accordance with the checking result.

14. (CANCELLED)

15. (PREVIOUSLY PRESENTED) A packet transfer control circuit incorporated in a first node to transfer a plurality of packets to a second node and a third node, in which the first node, the second node, and the third node are not connected in a ring form and each packet includes a data portion for storing data, the control circuit comprising:

a processor transferring a plurality of write packets, the data portion of which is blank, to each of the second and third nodes so that the second and third nodes substantially simultaneously store data in the data portion of the write packets received from the first node,

wherein the processor transfers to the second and third nodes a plurality of guide packets that store guide information indicating a state of the write packets before transferring the write packets from the first node to the second and third nodes, and

wherein the guide information written to the guide packets at the second and third nodes indicates that data has been written to the write packets by the second and third nodes, when the second and third nodes store the data in the data portion of the write packets received from the first node.

16. (CURRENTLY AMENDED) A packet transfer control circuit, comprising:

a processor as a first node among a plurality of nodes, which include the first node and a plurality of second nodes, not connected in a ring form and constitute an IEEE 1394 topology, transfers to the plurality of second nodes a packet determinable as a write packet at a data link layer processor of the plurality of second nodes, the data portion of which stores ~~data, and~~data, and then transferring another write packet, the data portion of which is blank, wherein each second node stores data in the blank data portion of the write packet wherein the processor

checks an identifier of the write packet received from an upstream node and determines whether data stored in data portion of the write packet can be replaced with another data stored in the packet transfer control circuit and to be addressed to the second nodes and replaces the data stored in the data portion of the write packet with the another data in accordance with the checking result.

17. (CANCELLED)

18. (PREVIOUSLY PRESENTED) A packet transfer control circuit incorporated in a first node to transfer packets to a plurality of second nodes, in which the first node and the plurality of second nodes are not connected in a ring form and each packet includes a data portion for storing data, the control circuit comprising:

a processor transferring to each second node a write packet, the data portion of which stores data, and then another write packet, the data portion of which is blank,

wherein each second node stores data in the blank data portion,

wherein the processor transfers to the second nodes guide packets that store guide information indicating a state of each write packet before transferring each write packet from the first node to the second nodes, and

wherein the guide information written to the guide packets at the second nodes indicates whether data has been written to each write packet by the second nodes, when each of the second nodes stores the data in the blank data portion of each write packet received from the first node.

19. (ORIGINAL) A packet transfer control circuit of a first network node, comprising

an input interface circuit for receiving a packet from a second network node connected to the first network node, the received packet being one of a normal packet type and a write packet type, and the received packet comprising at least a header portion and a data portion;

an input link layer processing circuit, connected to the input interface circuit, for receiving the received packet therefrom, reading the header portion of the packet to determine the packet type, and if the received packet is a normal packet, also determining an addressee of the packet;

an identification circuit, connected to the input link layer processing circuit, for receiving a write packet type of packet from the input link layer processing circuit, checking an identifier of the data portion of the write packet to determine whether the data portion of the write packet is

blank and to determine an addressee of the write packet, wherein the identification circuit generates a control signal if the data portion is blank;

a processor, connected to the identification circuit and the input link layer processing circuit, wherein the input link layer processing circuit passes the received packet directly to the processor if the received packet is addressed to the first node and is a normal type packet, wherein the processor receives the packet data from the identification circuit if the packet is a write type packet, and wherein the processor receives the control signal from the identification circuit and pads the data portion of the packet in order to fill the data portion of the packet when the control signal indicates that the data portion is blank;

a memory, connected to the processor, for storing the packet data processed by the processor;

an output link layer processing circuit, connected to the processor and to the input link layer processing circuit, for receiving the packet therefrom and preparing a transmission packet from the packet, wherein the input link layer processing circuit passes a normal type packet not addressed to the first node directly to the output link layer processing circuit; and

an output interface circuit, connected to the output link layer processing circuit, for receiving the transmission packet therefrom and transmitting the transmission packet over a bus to another node.

20. (ORIGINAL) The packet transfer control circuit of claim 19, wherein the packets are transferred between nodes over an IEEE 1394 compatible bus.

21. (ORIGINAL) The packet transfer control circuit of claim 19, further comprising:

an input physical layer processing circuit, connected between the input link layer processing circuit and the input interface circuit, for receiving the packets from the input interface circuit and transferring them to the input link layer processing circuit.

22. (ORIGINAL) The packet transfer control circuit of claim 21, further comprising:

an output physical layer processing circuit connected between the output link layer processing circuit and the output interface circuit, for transferring the transmission packet from the output link layer processing circuit to the output interface circuit.

23. (CURRENTLY AMENDED) A method, comprising:

transferring a write packet from a first node to a second node, when a plurality of nodes, including the first node, the second node and a third node, are connected in a star form and the plurality of nodes constitute an IEEE 1394 topology, the write packet having an identifier storing identification information which indicates addressee of data stored in data portion of the write packet or indicates that the data portion of the write packet includes a blank data portion;

determining at a link layer processor of the second node whether a received packet is the write packet;

checking at an identification circuit of the second node the identification information of the identifier of the received write packet and determining whether data stored in the data portion of the write packet can be replaced with another data stored in the second node and to be addressed to the third node;

storing data addressed to the third node and to be written in a data portion of a packet, in the data portion of the write packet at the second node in accordance with the checking result, wherein said storing data includes replacing the data stored in the data portion of the write packet with said another data; and

transferring the write packet from the second node to the third node.

24. (CURRENTLY AMENDED) A packet transfer control device, comprising:

a link layer processor as a first node to determine whether a received packet is a write packet, when a plurality of nodes, including the first node, a second node and a third node, are ~~not~~ connected in a ~~ring~~ star form and the plurality of nodes constitute an IEEE 1394 topology wherein the write packet has an identifier storing identification information which indicates addressee of data stored in data portion of the write packet or indicates that the data portion of the write packet includes a blank data portion;

an identification circuit connected to the link layer processor ~~to identify whether a data portion of the write packet received from the second node connected to the first node is blank~~ to check the identifier of the received write packet and determine whether data stored in the data portion of the write packet can be replaced with another data stored in the packet transfer control device and to be addressed to a downstream node; and

a host processor connected to the identification circuit ~~to determine whether data can be written to the data portion of the write packet, if the data portion of the write packet is blank according to the identifying by the identification circuit~~ to store data addressed to the downstream node to be written in a data portion of a packet, in the data portion of the received

write packet in accordance with the checking result of the identification circuit, wherein said storing includes replacing the data stored in the data portion of the received write packet with said another data, and transferring the write packet to the ~~third~~ downstream node.

25. (PREVIOUSLY PRESENTED) The packet transfer method according to claim 1, wherein the data comprises image data.

26. (PREVIOUSLY PRESENTED) The packet transfer method according to claim 23, wherein the data comprises image data.